1. **FLASH TYPE ADC**
   1. **OBJECTIVES**

To construct a FLASH type A to D Convertor using LTspice simulation.

* 1. **HARDWARE REQUIRED**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Equipment/Component name** | **Specifications/Value** | **Quantity** |
| 1 | LM324 | Refer data sheet in appendix | 1 |
| 3 | Resistors | 1K Ω | 8 |
| 5 | Dual Regulated power supply | (0 -30V), 1A | 1 |
| 5 | Regulated power supply | (0 -5V), 1A | 1 |
| 6 | Multimeter |  | 1 |

* 1. **THEORY**

A **flash ADC** (also known as a **direct-conversion ADC**) is a type of [analog-to-digital converter](https://en.wikipedia.org/wiki/Analog-to-digital_converter) that uses a linear [voltage ladder](https://en.wikipedia.org/wiki/Voltage_ladder) with a [comparator](https://en.wikipedia.org/wiki/Comparator) at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many [resistors](https://en.wikipedia.org/wiki/Resistor); however, modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital encoder, which converts the inputs into a binary value (the collected outputs from the comparators can be thought of as a [unary](https://en.wikipedia.org/wiki/Unary_numeral_system) value).Flash converters are extremely fast compared to many other types of ADCs, which usually narrow in on the "correct" answer over a series of stages. Compared to these, a flash converter is also quite simple and, apart from the analog comparators, only requires [logic](https://en.wikipedia.org/wiki/Digital_electronics) for the final conversion to [binary](https://en.wikipedia.org/wiki/Binary_numeral_system). For best accuracy, often a [track-and-hold](https://en.wikipedia.org/wiki/Sample_and_hold) circuit is inserted in front of the ADC input. This is needed for many ADC types (like [successive approximation ADC](https://en.wikipedia.org/wiki/Successive_approximation_ADC)), but for flash ADCs there is no real need for this, because the comparators are the sampling devices.

A flash converter requires a huge number of [comparators](https://en.wikipedia.org/wiki/Comparator) compared to other ADCs, especially as the precision increases. A flash converter requires {\displaystyle 2^{n}-1}comparators for an *n*-bit conversion. The size, power consumption and cost of all those comparators makes flash converters generally impractical for precisions much greater than 8 bits (255 comparators). In place of these comparators, most other ADCs substitute more complex [logic](https://en.wikipedia.org/wiki/Digital_circuit) and/or analog circuitry that can be scaled more easily for increased [precision](https://en.wikipedia.org/wiki/Accuracy_and_precision). Flash ADCs have been implemented in many technologies, varying from silicon-based [bipolar](https://en.wikipedia.org/wiki/Bipolar_junction_transistor) (BJT) and complementary metal–oxide [FETs](https://en.wikipedia.org/wiki/Field-effect_transistor) ([CMOS](https://en.wikipedia.org/wiki/CMOS)) technologies to rarely used [III-V](https://en.wikipedia.org/wiki/List_of_semiconductor_materials) technologies. Often this type of ADC is used as a first medium-sized analog circuit verification.

The earliest implementations consisted of a reference ladder of well-matched resistors connected to a reference voltage. Each tap at the [resistor ladder](https://en.wikipedia.org/wiki/Resistor_ladder) is used for one comparator, possibly preceded by an [amplification](https://en.wikipedia.org/wiki/Amplifier) stage, and thus generates a logical 0 or 1 depending on whether the measured voltage is above or below the [reference voltage](https://en.wikipedia.org/w/index.php?title=Reference_voltage&action=edit&redlink=1) of the [resistor tap](https://en.wikipedia.org/w/index.php?title=Resistor_tap&action=edit&redlink=1). The reason to add an amplifier is twofold: it amplifies the voltage difference and therefore suppresses the comparator offset, and the kick-back noise of the comparator towards the reference ladder is also strongly suppressed. Typically designs from 4-bit up to 6-bit and sometimes 7-bit are produced.

Designs with power-saving capacitive reference ladders have been demonstrated. In addition to clocking the comparator(s), these systems also sample the reference value on the input stage. As the sampling is done at a very high rate, the leakage of the capacitors is negligible. Recently offset calibration has been introduced into flash ADC designs. Instead of high-precision analog circuits (which increase component size to suppress variation) comparators with relatively large offset errors are measured and adjusted. A test signal is applied, and the offset of each comparator is calibrated to below the [LSB](https://en.wikipedia.org/wiki/Least_significant_bit) value of the ADC.

Another improvement to many flash ADCs is the inclusion of digital error correction. When the ADC is used in harsh environments or constructed from very small integrated circuit processes, there is a heightened risk that a single comparator will randomly change state resulting in a wrong code. Bubble error correction is a digital correction mechanism that prevents a comparator that has, for example, tripped high from reporting logic high if it is surrounded by comparators that are reporting logic low.

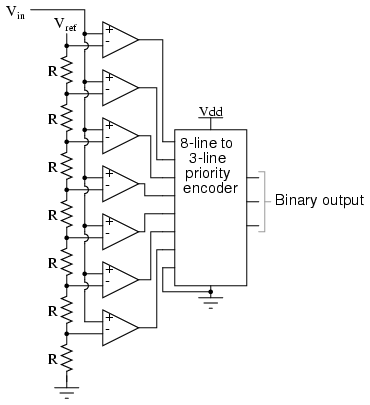


Fig: 1 Flash type ADC

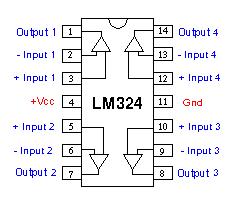


Fig: 2 IC pin configuration LM324

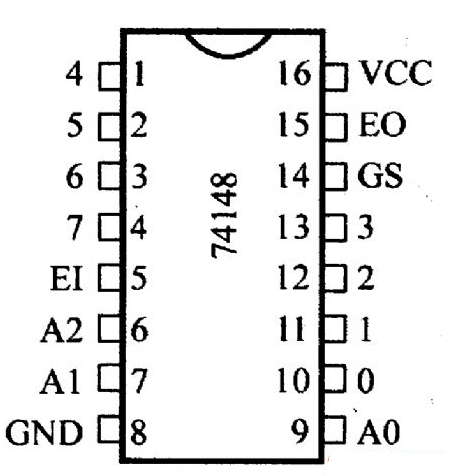


Fig: 3 IC pin configuration 74LS148

**Flash type ADC**

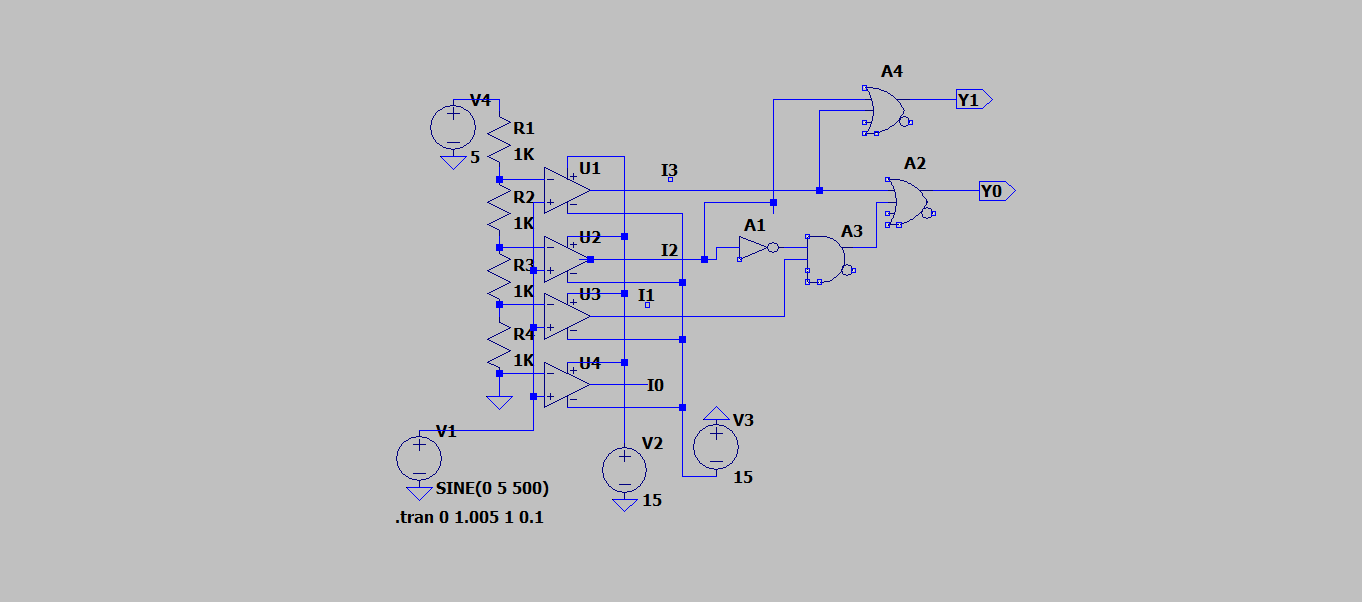
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Analog i/p**  **(0-5v)** | **Comparator o/p** | | | | | | | | **Digital o/p** | | | **Analog i/p**  **Observed (v)** |
| **\_**  **I7** | **\_**  **I6** | **\_**  **I5** | **\_**  **I4** | **\_**  **I3** | **\_**  **I2** | **\_**  **I1** | **\_**  **I0** | **\_**  **A2** | **\_**  **A1** | **\_**  **A0** |
| **0-0.5** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** |  |
| **0.5-1.0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **1** |  |
| **1.0-1.5** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **1** | **0** |  |
| **1.5-2.0** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** |  |
| **2.0-2.5** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **0** | **0** |  |
| **2.5-3.0** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** |  |
| **3.-3.5** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** |  |
| **3.5-4.0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |  |

**Design Constraints**

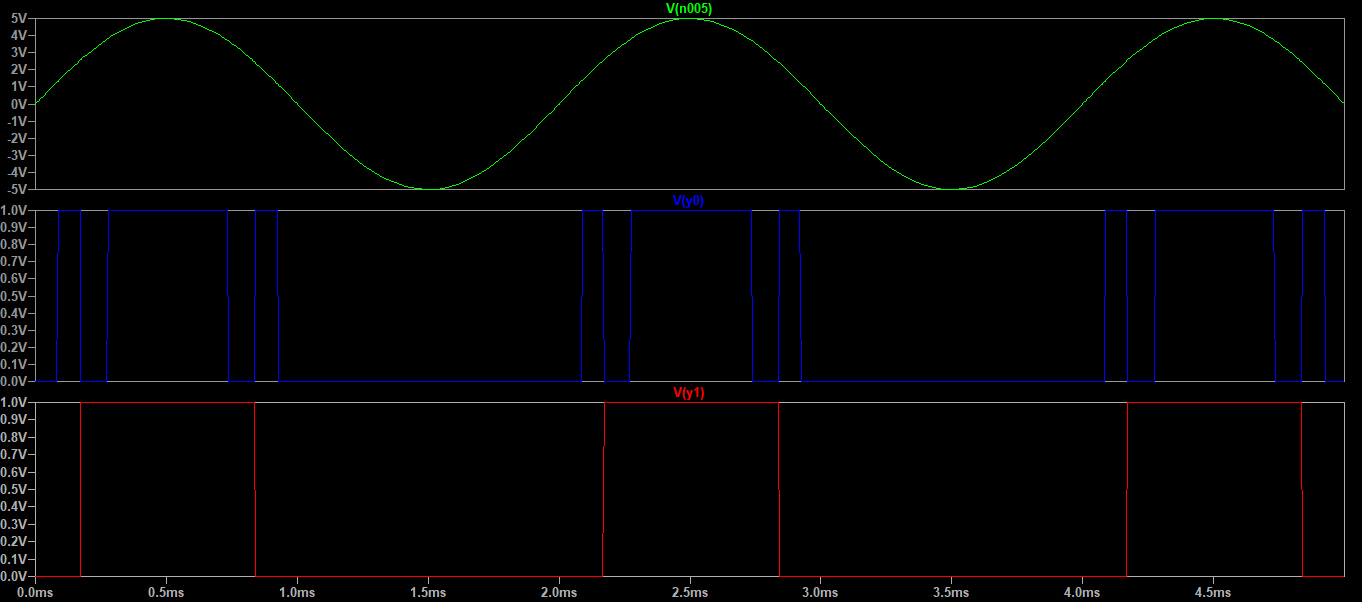
* Resistance should be use ±1 to ±5 tolerance
* Input voltage should be 5V for high and 0V for low.

**13.4 LTSPICE SIMULATION**

**Circuit Diagram:**



**Input and Output:**



**Observation:**

|  |  |  |
| --- | --- | --- |
| **Input voltage range** | **Output** | |
|  |  |
| 0 to 1.25 V |  |  |
| 1.25 V to 2.5 V |  |  |
| 2.5 V to 3.75 V |  |  |
| 3.75 V to 5 V |  |  |

**13.5 PRE LAB QUESTIONS**

1. Classify ADCs on the basis of their output.
2. Mention the control lines present in ADC.
3. Which type of ADC follows conversion technique of changing the analog input voltage as a function of frequency?

**13.6 POST LAB QUESTIONS**

1. Calculate the conversion time of a 12-bit counter type ADC with 1MHz clock frequent to convert a full scale input?
2. How many comparators are required for 4-bit ADC?

**Result:**